

FEATURES

Isolation Test Voltage: To 3.5 kV rms
Five Isolated Logic Lines: Available in Six I/O Configurations
Logic Signal Bandwidth: 20 MHz (min)
CMV Transient Immunity: 10 kV/ μ s min
Waveform Edge Transmission Symmetry: ± 1 ns
Field and System Output Enable/Three-State Functions
Performance Rated Over -25°C to +85°C
UL1950, IEC950, EN60950 Certification (VDE, CE, Pending)

APPLICATIONS

PLC/DCS Analog Input and Output Cards
Communications Bus Isolation
General Data Acquisition Applications
IGBT Motor Drive Controls
High Speed Digital I/O Ports

GENERAL DESCRIPTION

The AD 261 is designed to isolate five digital control signals to/from a microcontroller and its related field I/O components. Six models allow all I/O combinations from five input lines to five output lines, including combinations in between. Every AD 261 effectively replaces up to five opto-isolators.

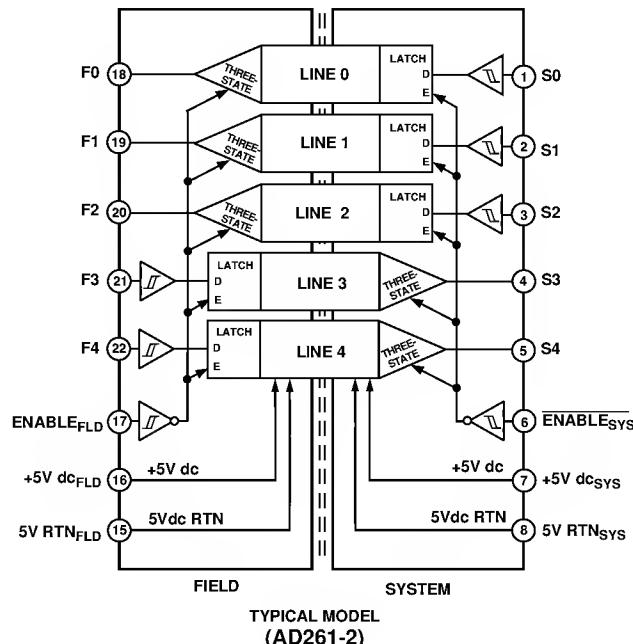
Each line of the AD 261 has a bandwidth of 20 MHz (min) with a propagation delay of only 14 ns, which allows for extremely fast data transmission. Output waveform symmetry is maintained to within ± 1 ns of the input so the AD 261 can be used to accurately isolate time-based PWM signals.

All field or system output pins of the AD 261 can be set to a high resistance three-state level by use of the two enable pins. A field output three-stated offers a convenient method of presetting logic levels at power-up by use of pull-up/down resistors. System side outputs being three-stated allows for easy multiplexing of multiple AD 261s.

The isolation barrier of the AD 261 B Grade is 100% tested as high as 3.5 kV rms (system to field). The barrier design also provides excellent common-mode transient immunity from 10 kV/ μ s common-mode voltage excursions of field side terminals relative to the system side, with no false output triggering on either side.

Each output is updated within nanoseconds by input logic transitions, the AD 261 also has a continuous output update feature that automatically updates each output based on the dc level of the input. This guarantees the output is always valid 10 μ s after a fault condition or after the power-up reset interval.

FUNCTIONAL BLOCK DIAGRAM



PRODUCT HIGHLIGHTS

Six Isolated Logic Line I/O Configurations Available The AD 261 is available in six pin-compatible versions of I/O configurations to meet a wide variety of requirements.

Wide Bandwidth with Minimal Edge Error: The AD 261 affords extremely fast isolation of logic signals due to its 20 MHz bandwidth and 14 ns propagation delay. It maintains a waveform input-to-output edge transition error of typically less than ± 1 ns (total) for positive vs. negative transition.

3.5 kV rms Test Voltage Isolation Rating: The AD 261 B Grade is rated to operate at 1.25 kV rms and is 100% production tested at 3.5 kV rms, using a standard ADI test method.

High Transient Immunity: The AD 261 rejects common-mode transients slewing at up to 10 kV/ μ s without false triggering or damage to the device.

(Continued on page 5)

REV. 0

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AD261- SPECIFICATIONS

(Typical at $T_A = +25^\circ\text{C}$, $+5 \text{ V dc}_{\text{SYS}}$, $+5 \text{ V dc}_{\text{FLD}}$, $t_{\text{RR}} = 50 \text{ ns max}$ unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS					
Threshold Voltage					
Positive T transition (V_{T+})	$+5 \text{ V dc}_{\text{SYS}} = 4.5 \text{ V}$ $+5 \text{ V dc}_{\text{SYS}} = 5.5 \text{ V}$	2.0	2.7	3.15	V
Negative T transition (V_{T-})	$+5 \text{ V dc}_{\text{SYS}} = 4.5 \text{ V}$ $+5 \text{ V dc}_{\text{SYS}} = 5.5 \text{ V}$	0.9	1.8	2.2	V
Hysteresis Voltage (V_H)	$+5 \text{ V dc}_{\text{SYS}} = 4.5 \text{ V}$ $+5 \text{ V dc}_{\text{SYS}} = 5.5 \text{ V}$	1.2	2.2	3.0	V
Input Capacitance (C_{IN})	$+5 \text{ V dc}_{\text{SYS}} = 4.5 \text{ V}$	0.4	0.9	1.4	V
Input Bias Current (I_{IN})	$+5 \text{ V dc}_{\text{SYS}} = 5.5 \text{ V}$	0.5	1.0	1.5	V
	Per Input		5		pF
			0.5		μA
OUTPUT CHARACTERISTICS					
Output Voltage ¹					
High Level (V_{OH})	$+5 \text{ V dc}_{\text{SYS}} = 4.5 \text{ V}, I_O = 0.02 \text{ mA}$ $+5 \text{ V dc}_{\text{SYS}} = 4.5 \text{ V}, I_O = 4 \text{ mA}$	4.4			V
Low Level (V_{OL})	$+5 \text{ V dc}_{\text{SYS}} = 4.5 \text{ V}, I_O = 0.02 \text{ mA}$ $+5 \text{ V dc}_{\text{SYS}} = 4.5 \text{ V}, I_O = 4 \text{ mA}$	3.7			V
Output Three-State Leakage Current	ENABLE $E_{\text{SYS/FLD}}$ @ Logic Low/High Level Respectively		0.1		V
			0.4		V
		0.5			μA
DYNAMIC RESPONSE ² (Refer to Figure 2)					
Max Logic Signal Frequency (f_{MIN})	50% Duty Cycle, $+5 \text{ V dc}_{\text{SYS}} = 5 \text{ V}$	20			MHz
Waveform Edge Symmetry Error (t_{ERROR})	t_{PHL} vs. t_{PLH}	± 1			ns
Logic Edge Propagation Delay ($t_{\text{PHL}}, t_{\text{PLH}}$)		14		25	ns
Minimum Pulsewidth (t_{PWMIN})		25			ns
Max Output Update Delay on Fault or After Power-Up Reset Interval ($\approx 30 \mu\text{s}$) ²			12		μs
ISOLATION BARRIER RATING ³					
Operating Isolation Voltage (V_{CMV})	AD 261A AD 261B		375		V rms
Isolation Rating Test Voltage ($V_{\text{CMV TEST}}$) ⁴	AD 261A AD 261B	1750	1250		V rms
Transient Immunity ($V_{\text{TRANSIENT}}$)	Total Capacitance, All Lines	3500			V rms
Isolation Mode Capacitance (C_{ISO})	240 V rms @ 60 Hz	10,000			V rms
Capacitive Leakage Current (I_{LEAD})		9	15		$\text{V}/\mu\text{s}$
			2		pF
					μA rms
POWER SUPPLY					
Supply Voltage (+5 V dc _{SYS} and +5 V dc _{FLD})	Rated Performance Operating	4.5	5.5		V dc
Power Dissipation Capacitance	Effective, per Input, Either Side	4.0	5.75		V dc
Quiescent Supply Current	Effective per Output, Either Side—No Load	8			pF
Supply Current	Each, +5 V dc _{SYS & FLD}	28			pF
	All Lines @ 10 MHz (Sum of +5 V dc _{SYS & FLD})	4			mA
		18			mA
TEMPERATURE RANGE					
Rated Performance (T_A) ⁵		-25		+85	°C
Storage (T_{STG})		-40		+85	°C

NOTES

¹For best performance, bypass +5 V dc supplies to com., at or near the device (0.01 μF). +5 V dc supplies are also internally bypassed with 0.05 μF .

²As the supply voltage is applied to either side of the AD 261, the internal circuitry will go into a power-up reset mode (all lines disabled) for about 30 μs after the point where +5 V dc_{SYS & FLD} passes above 3.3 V.

³"Operating" isolation voltage is derived from the Isolation Test Voltage in accordance with such methods as found in VDE-0883 wherein a device will be "hi-pot" tested at twice the operating voltage, plus one thousand volts. Partial discharge testing, with an acceptance threshold of 80 pC of discharge may be considered the same as a hi-pot test (but nondestructive).

⁴Partial Discharge at 80 pC THLD.

⁵Supply Current will increase slightly, but otherwise the unit will function within specification to -40°C.

Specifications are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Parameter	Conditions	Min	Typ	Max	Units
Supply Voltage (+5 V dc _{SYS & FLD})		-0.5	+6.0	+6.0	V
DC Input Voltage (V _{IN MAX})	Referred to +5 V dc _{SYS & FLD} and 5 V RTN _{SYS & FLD} Respectively	-0.5	+0.5	+0.5	V
DC Output Voltage (V _{OUT MAX})	Referred to +5 V RTN _{SYS & FLD} and 5 V dc _{SYS & FLD} Respectively	-0.5	+0.5	+0.5	V
Clamp Diode Input Current (I _{IK})	For V _I < -0.5 V or V _I > 5 V RTN _{SYS & FLD} +0.5 V	-25	+25	+25	mA
Clamp Diode Output Current (I _{OK})	For V _O < -0.5 V or V _O > 5 V RTN _{SYS & FLD} +0.5 V	-25	+25	+25	mA
Output DC Current, per Pin (I _{OUT})		-25	+25	+25	mA
DC Current, V _{CC} or GND (I _{CC} or I _{GND})		-50	+50	+50	mA
Storage Temperature (T _{STG})		-40	+85	+85	°C
Lead Temperature (Soldering, 10 sec)				+300	°C
Electrostatic Protection (V _{ESD})	Per MIL-STD-883, Method 3015	4.5	5		kV

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may effect device reliability.

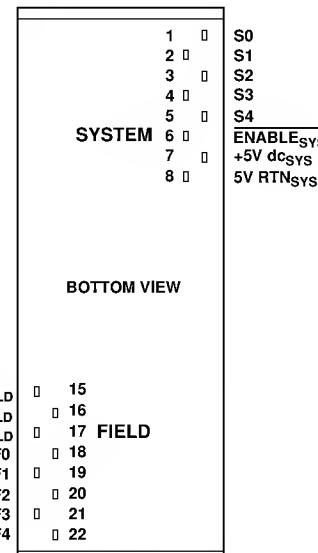
I/O CONFIGURATIONS AVAILABLE

The AD 261 is available in several configurations. The choice of model is determined by the desired number of input vs. output lines. All models have identical footprints with the power and enable pins always being in the same locations.

PIN FUNCTION DESCRIPTIONS

Pin	Mnemonic	Function
1-5*	S0 T through S4	Digital Xmt or Rcv from F0 T through F4
6	ENABLE _{SYS}	System Output Enable/Three-State
7	+5 V dc _{SYS}	System Power Supply (+5 V dc Input)
8	5 V RTN _{SYS}	System Power Supply Common
9-14		Not Present On Unit
15	5 V RTN _{FLD}	Field Power Supply Common
16	+5 V dc _{FLD}	Field Power Supply (+5 V Input)
17	ENABLE _{FLD}	Field Output Enable/Three-State
18-22*	F0 T through F4	Digital Xmt or Rcv from S0 T through S4

*Function of pin determined by model. Refer to Table I.

PIN CONFIGURATION**ORDERING GUIDE**

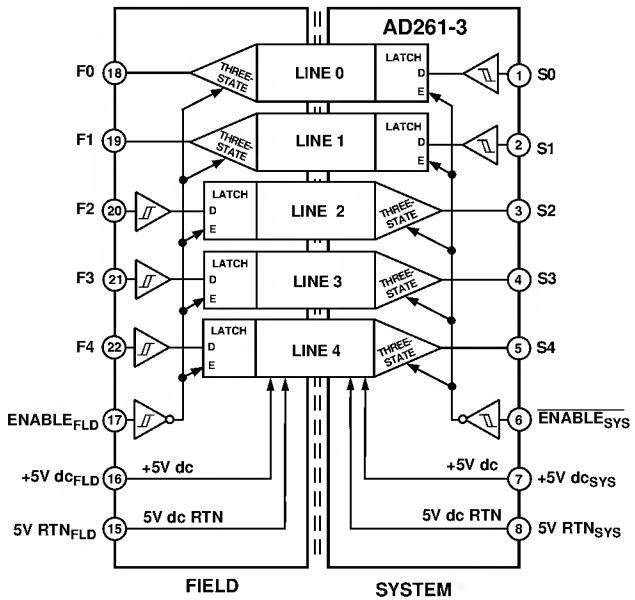
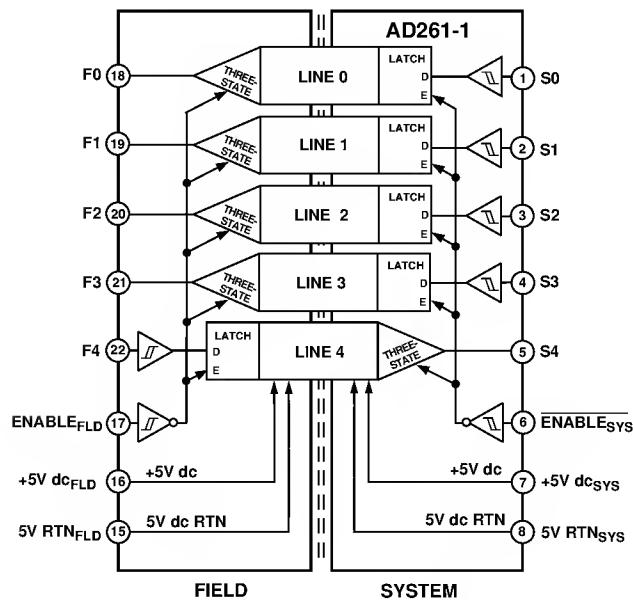
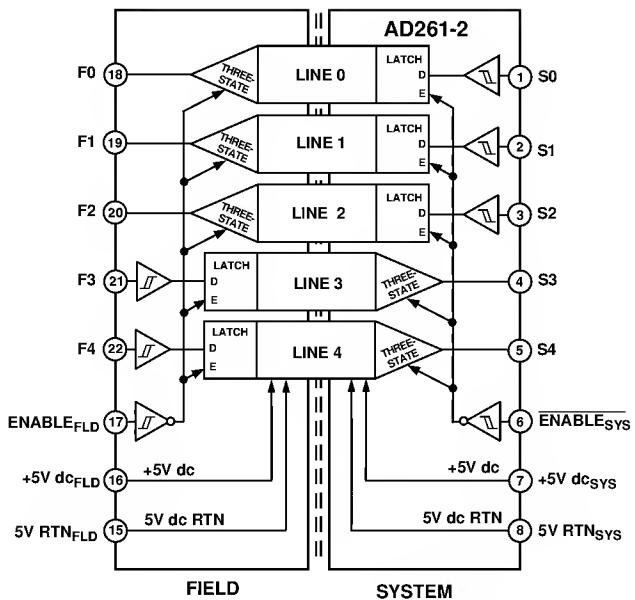
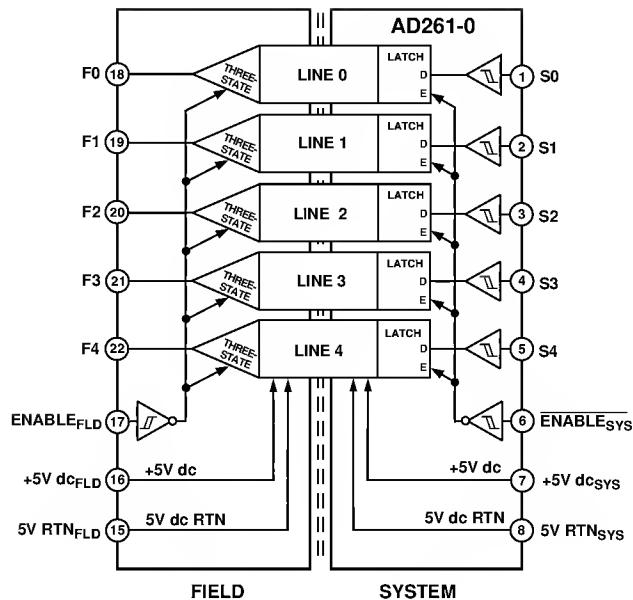
Model Number	Description	Isolation Ratings	Package Description	Package Option
AD261AND-0	0 Inputs, 5 Outputs	1.75 kV rms	Plastic DIP	ND-22A
AD261AND-1	1 Input, 4 Outputs	1.75 kV rms	Plastic DIP	ND-22A
AD261AND-2	2 Inputs, 3 Outputs	1.75 kV rms	Plastic DIP	ND-22A
AD261AND-3	3 Inputs, 2 Outputs	1.75 kV rms	Plastic DIP	ND-22A
AD261AND-4	4 Inputs, 1 Output	1.75 kV rms	Plastic DIP	ND-22A
AD261AND-5	5 Inputs, 0 Outputs	1.75 kV rms	Plastic DIP	ND-22A
AD261BND-0	0 Inputs, 5 Outputs	3.5 kV rms	Plastic DIP	ND-22A
AD261BND-1	1 Input, 4 Outputs	3.5 kV rms	Plastic DIP	ND-22A
AD261BND-2	2 Inputs, 3 Outputs	3.5 kV rms	Plastic DIP	ND-22A
AD261BND-3	3 Inputs, 2 Outputs	3.5 kV rms	Plastic DIP	ND-22A
AD261BND-4	4 Inputs, 1 Output	3.5 kV rms	Plastic DIP	ND-22A
AD261BND-5	5 Inputs, 0 Outputs	3.5 kV rms	Plastic DIP	ND-22A

CAUTION

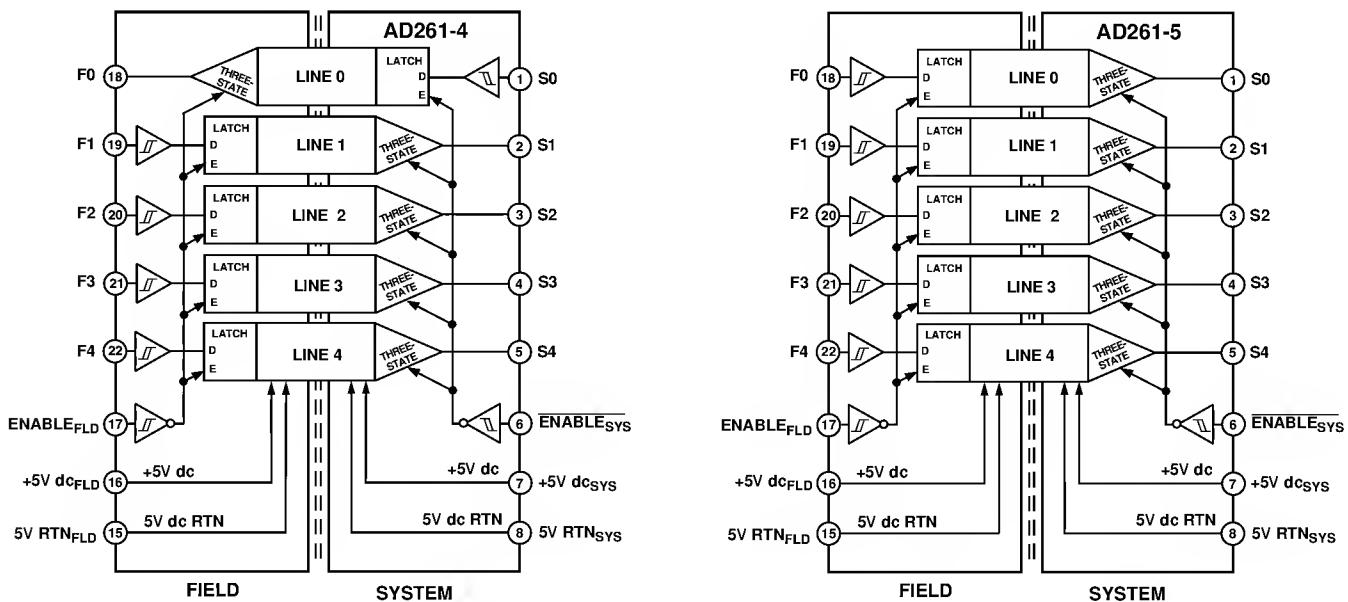
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD 261 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



AD261 CONFIGURATIONS



AD261 CONFIGURATIONS



(Continued from page 1)

Field and System Enable Functions: Both the isolated and nonisolated sides of the AD 261 have ENABLE pins that three-state all outputs. Upon reenabling these pins, all outputs are updated to reflect the current input logic level.

CE Certifiable Simply by adding the external bypass capacitors at the supply pins, the AD 261 can attain CE certification in most applications (to the EMC directive) and conformance to the low voltage (safety) directive is assured by the EN 60950 certification.

Table I. Model Number and Pinout Function

Pin	AD 261-0	AD 261-1	AD 261-2	AD 261-3	AD 261-4	AD 261-5
1	S0 (X mt)	S0 (X mt)	S0 (X mt)	S0 (X mt)	S0 (Rcv)	
2	S1 (X mt)	S1 (X mt)	S1 (X mt)	S1 (X mt)	S1 (Rcv)	
3	S2 (X mt)	S2 (X mt)	S2 (X mt)	S2 (Rcv)	S2 (Rcv)	
4	S3 (X mt)	S3 (X mt)	S3 (Rcv)	S3 (Rcv)	S3 (Rcv)	
5	S4 (X mt)	S4 (Rcv)	S4 (Rcv)	S4 (Rcv)	S4 (Rcv)	
6	ENABLE _{SYS}	*	*	*	*	*
7	+5 V dc _{SYS}	*	*	*	*	*
8	5 V RTN _{SYS}	*	*	*	*	*
9-14		Not Present				
15	5 V RTN _{FLD}	*	*	*		*
16	+5 V dc _{FLD}	*	*	*	*	*
17	ENABLE _{FLD}	*	*	*	*	*
18	F0 (Rcv)	F0 (Rcv)	F0 (Rcv)	F0 (Rcv)	F0 (X mt)	
19	F1 (Rcv)	F1 (Rcv)	F1 (Rcv)	F1 (Rcv)	F1 (X mt)	
20	F2 (Rcv)	F2 (Rcv)	F2 (Rcv)	F2 (X mt)	F2 (X mt)	
21	F3 (Rcv)	F3 (Rcv)	F3 (X mt)	F3 (X mt)	F3 (X mt)	
22	F4 (Rcv)	F4 (X mt)	F4 (X mt)	F4 (X mt)	F4 (X mt)	

*Pin function is the same on all models, as shown in the AD 261-0 column.

GENERAL ATTRIBUTES

The AD 261 provides five HCMOS compatible isolated logic lines with $\geq 10 \text{ kV}/\mu\text{s}$ common-mode transient immunity.

The case design and pin arrangement provides greater than 18 mm spacing between field and system side conductors, providing CSA/IS and IEC creepage spacing consistent with 750 V mains isolation.

The five unidirectional logic lines have six possible combinations of "ins" and "outs," or transmitter/receiver pairs; hence there are six AD 261 part configurations (see Table I).

Each 20 MHz logic line has a Schmidt trigger input and a three-state output (on the other side of the isolation barrier) and 14 ns of propagation delay. A single enable pin on either side of the barrier causes all outputs on that side to go three-state and all inputs (driven pins) to ignore their inputs and retain their last known state.

Note: All unused logic inputs (1-5) should be tied either high or low, but not left floating.

Edge "fidelity," or the difference in propagation time for rising and falling edges, is typically less than $\pm 1 \text{ ns}$.

Power consumption, unlike opto-isolators, is a function of operating frequency. Each logic line barrier driver requires about 160 μA per MHz and each receiver 40 μA per MHz plus, of course, 4 mA total idle current (each side). The supply current diminishes slightly with increasing temperature (about $-0.03\%/\text{C}$).

The total capacitance spanning the isolation barrier is less than 10 pF.

The minimum period of a pulse that can be accurately coupled across the barrier is about 25 ns. Therefore the maximum square-wave frequency of operation is 20 MHz.

AD261

Logic information is sent across the barrier as "set-hi/set-lo" data that is derived from logic level transitions of the input. At power-up or after a fault condition, an output might not represent the state of the respective channel input to the isolator. An internal circuit operates in the background which interrogates all inputs about every 5 μ s and in the absence of logic transitions, sends appropriate "set-hi" or "set-lo" data across the barrier.

Recovery time from a fault condition or at power-up is thus between 5 μ s and 10 μ s.

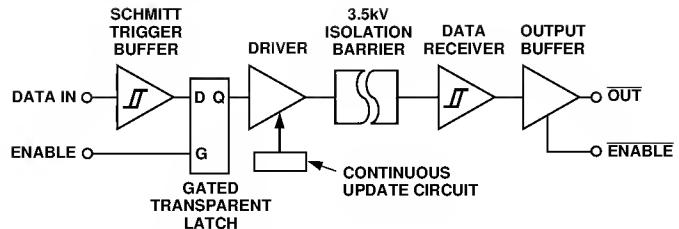


Figure 1. Simplified Block Diagram

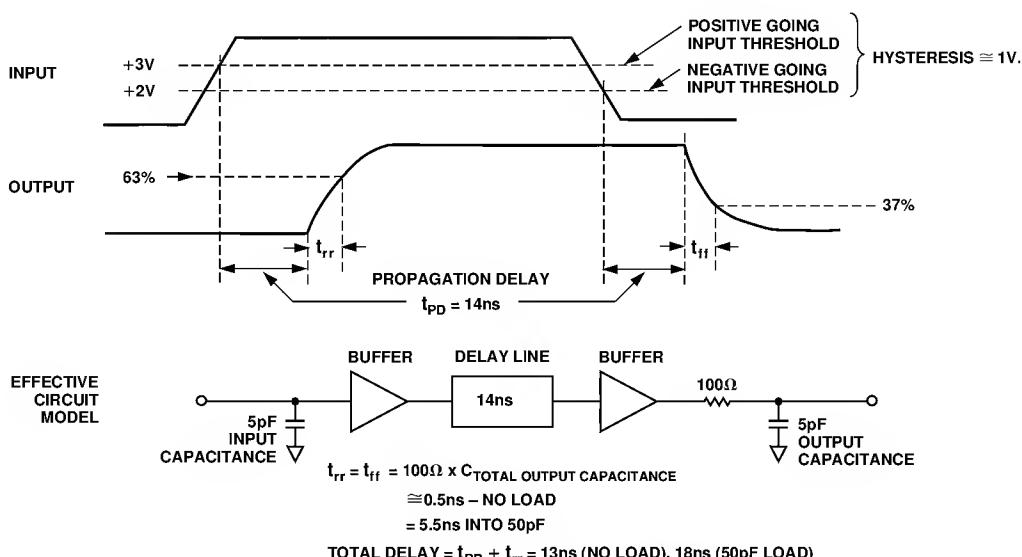
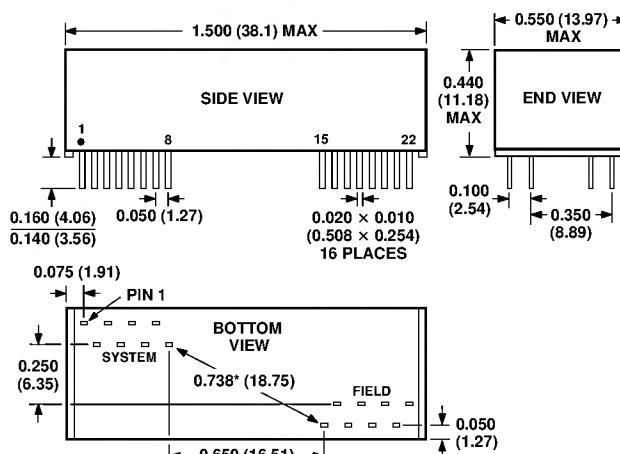


Figure 2. Typical Timing and Delay Models

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

22-Pin Plastic DIP (ND-22A)



*CREEPAGE PATH (SUBTRACT APPROXIMATELY 0.079 (2mm) FOR SOLDER PAD RADII ON PC BOARD.
THIS SPACING SUPPORTS THE INTRINSICALLY SAFE RATING OF 750V.